N32G003x5

N32G003 32 bit ARM Cortex-M0 48MHz 29.5KB Flash 3KB SRAM 1x12bit 1Msps ADC 1xCOMP 2xUART 1xI2C 1xSPI

CPU

32 ARM Cortex-M0

48MHz

29.5KByte Flash 10 10

3KByte SRAM

Run

Stop TIM6 IWDG SRAM IO

Power Down NRST PA1_WKUP0 PA2_WKUP

HSI RC OSC 48MHz/40MHz

LSI RC OSC 32KHz

1 HSI LSI

/ /

2 UART

1 SPI 12MHz

1 I2C 1MHz

1 12bits 1Msps ADC 9 1 1.2V

1 0mV/ 100mV/ 200mV/ 300mV

18 GPIOs.

1

1 16bit 4 3

6 PWM

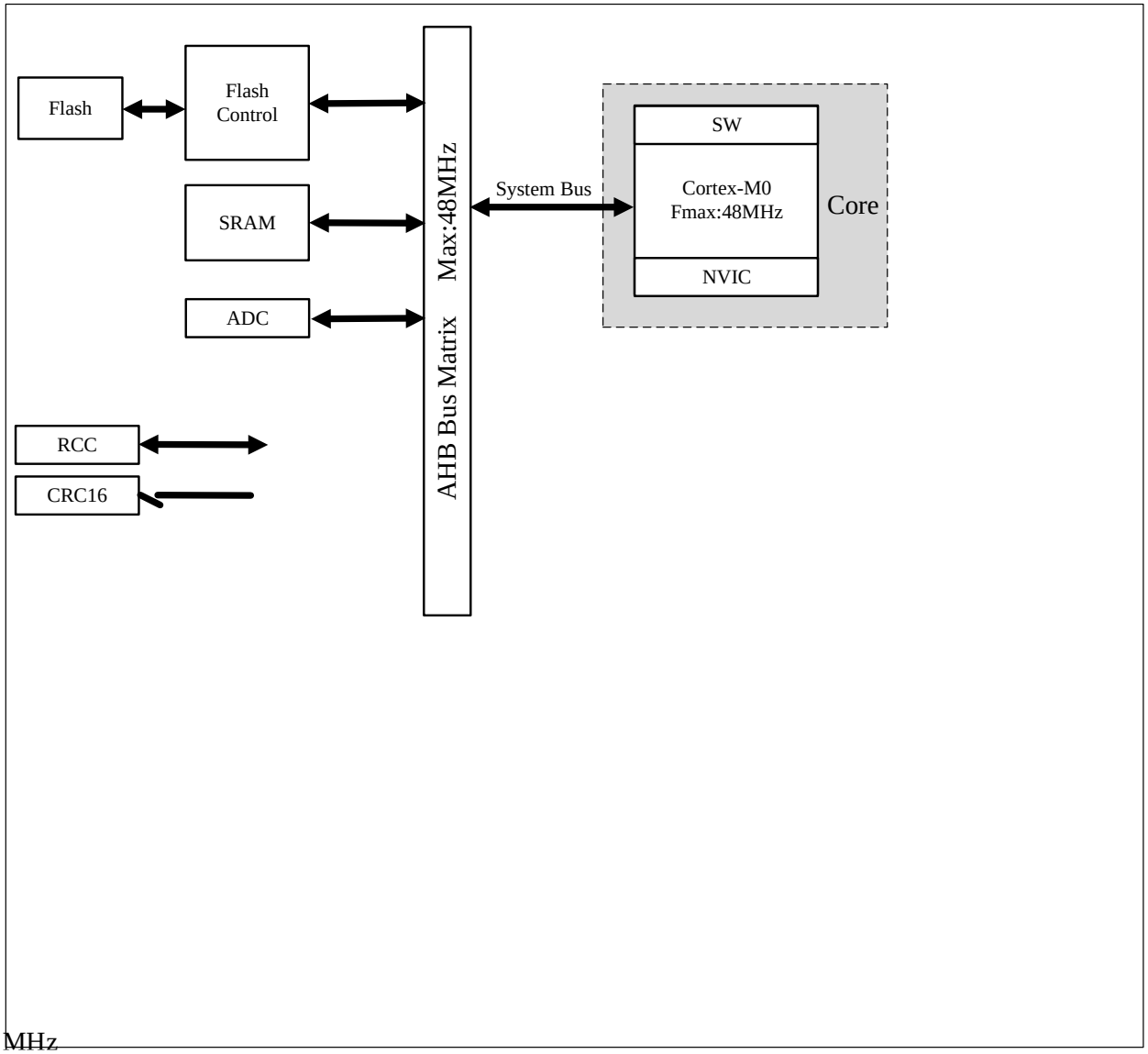
1

N32G003 32 ARM Cortex®-M0 48MHz 29.5KB
Flash 3KB SRAM AHB APB
18 I/O 1 12 1Msps ADC 9 1
2 UART 1 I2C 1 SPI

N32G003 -40℃ +105℃ 1.8V 5.5V
20

N32G003
1-1

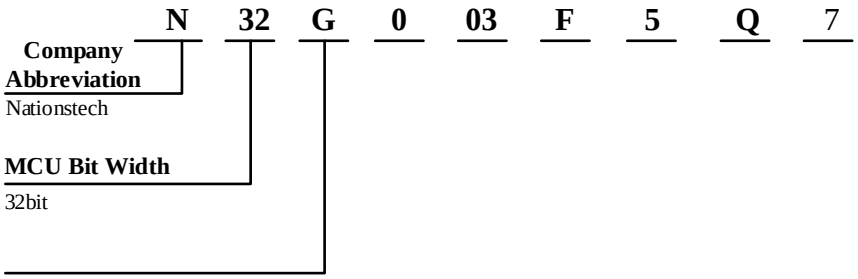
1-1 N32G003



MHz

1.1

1-2 N32G003



1.2

1-1 N32G003

	N32G003F5Q7	N32G003F5S7
Flash		

2

2.1

N32G003 ARM Cortex®-M0

2.2

N32G003 Flash SRAM 2-1

2-1

2.2.1

29.5K FLASH 512byte

NVIC

16 16 Cortex®-M0

4 2

2.3 / (EXTI)

/ 20 /

3

2-2

(PVD) V_{DD} V_{PVD} V_{DD}

2.9.2 (TIM3)

TIM3

16 /

16 1 65536

TIM3 2

PWM

TIM1_CC5

2.9.4 **(Systick)**

24

I2C

/ (ACK)

PEC( )

PEC

PEC

2.11 (UART)

N32G003 2 (UART1 UART2)

UART1 UART2

UART

NRZ

8-bit 9-bit

1-bit 2-bit

8

UART modes	UART1	USART2
( )		

2.12 (SPI)

1 SPI SPI /

GPIO

I/O I/O 32 16 8

2.14 / (ADC)

12 ADC 10 9 1
A/D ADC / 16
/ ADC
24MHz

ADC

1 ADC 9 1

12 1MSPS

ADC

HSI ADC_CLK 48M

HSI ADC_1MCLK 1MHz

Blanking Blanking

(BEEPER)

BEEPER

2.17 (CRC)

CRC16 (CRC) CRC
CRC

CRC

CRC16 $X^{16}+X^{15}+X^{2}+X^{0}$

CRC16 1 AHB HCLK

(UID)

N32G003 96 UID(Unique device ID) 128
UCID(Unique Customer ID)
N32G003
CPU SWD

UID 96

UCID 128

2.19 SWD (SWD)

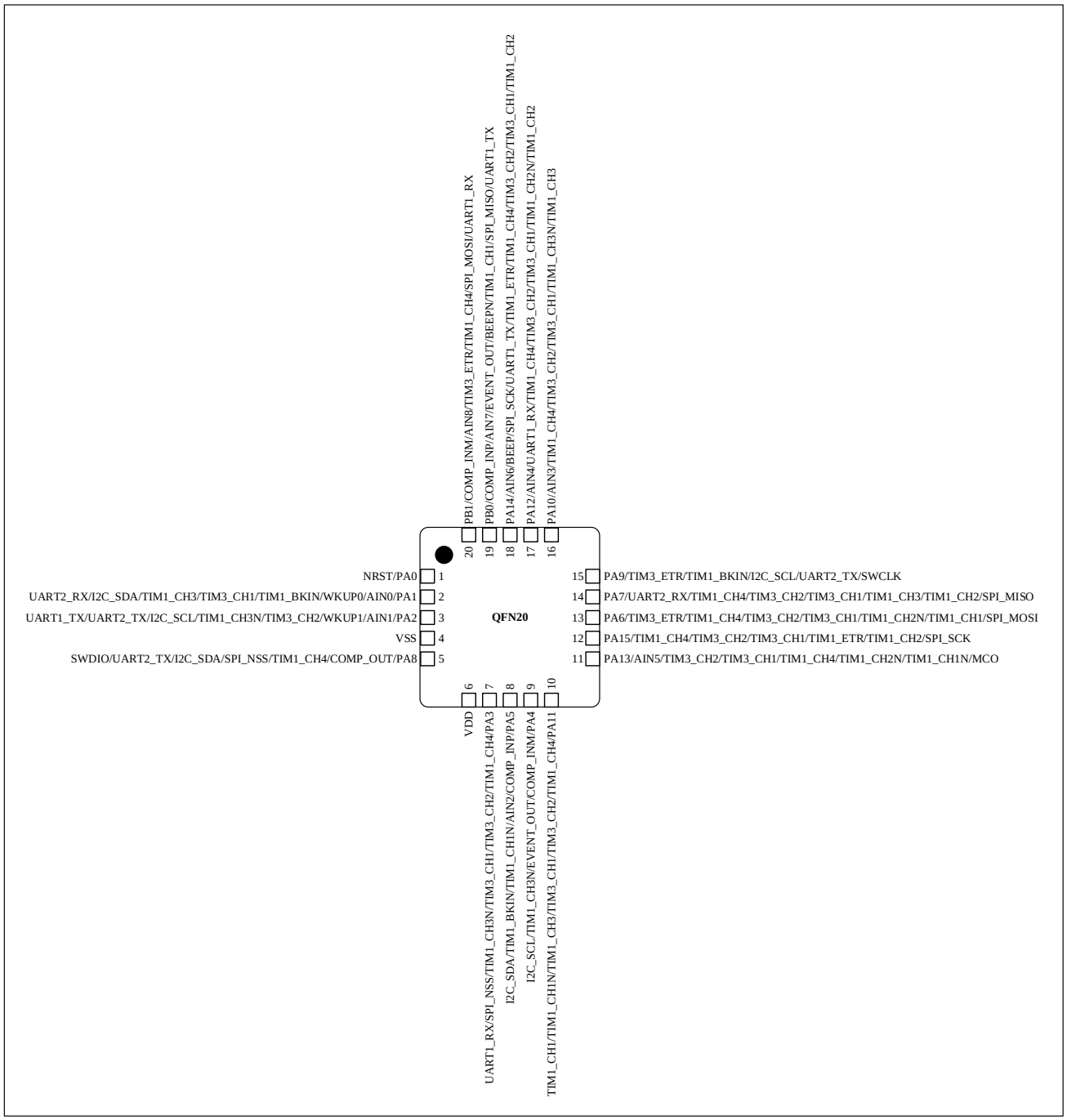
ARM SWD

3

3.1

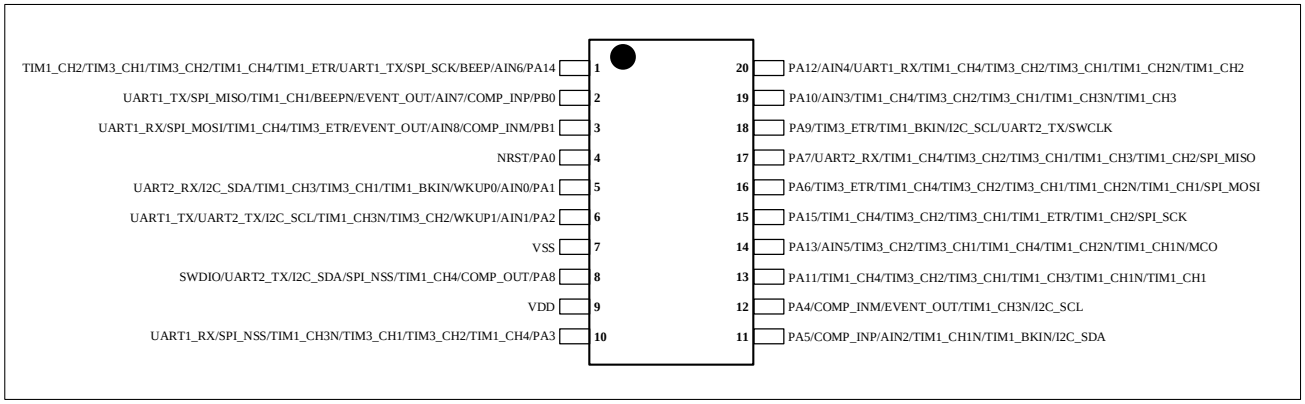
N003 QFN20

3-1 N32G003 QFN20



3.1.2 TSSOP20

3-2 N32G003 TSSOP20



8	5	PA8[3] (SWDIO)	I/O	SWDIO UART2_TX I2C_SDA SPI_NSS TIM1_CH4 COMP_OUT	-
9	6	VDD	S	VDD	-
10	7	PA3	I/O	UART1_RX SPI_NSS TIM1_CH3N TIM3_CH1 TIM3_CH2 TIM1_CH4	-
11	8	PA5	I/O	I2C_SDA TIM1_BKIN TIM1_CH1N	AIN2 COMP_INP
12	9	PA4	I/O	I2C_SCL TIM1_CH3N EVENT_OUT	COMP_INM
13	10	PA11	I/O	TIM1_CH1 TIM1_CH1N TIM1_CH3 TIM3_CH1 TIM3_CH2 TIM1_CH4	-
14	11	PA13	I/O	MCO TIM1_CH1N TIM1_CH2N TIM1_CH4 TIM3_CH1 TIM3_CH2	AIN5
15	12	PA15	I/O	SPI_SCK TIM1_CH2 TIM1_ETR TIM3_CH1 TIM3_CH2 TIM1_CH4	-

16	13	PA6	I/O	SPI_MOSI TIM1_CH1 TIM1_CH2N TIM3_CH1 TIM3_CH2 TIM1_CH4 TIM3_ETR	-
17	14	PA7	I/O	SPI_MISO TIM1_CH2 TIM1_CH3 TIM3_CH1 TIM3_CH2 TIM1_CH4 UART2_RX	-
18	15	PA9[3] (SWCLK)	I/O	SWCLK UART2_TX I2C_SCL TIM1_BKIN TIM3_ETR	-

4

4.1

V_{SS}

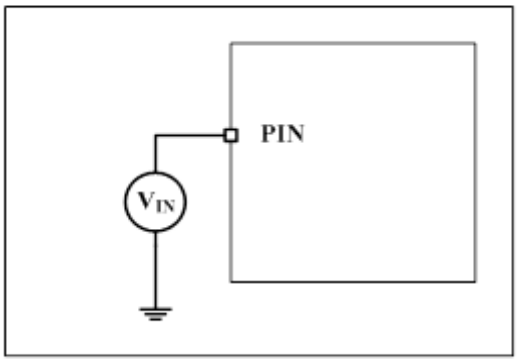
4.1.1

100% T_A=25℃

/

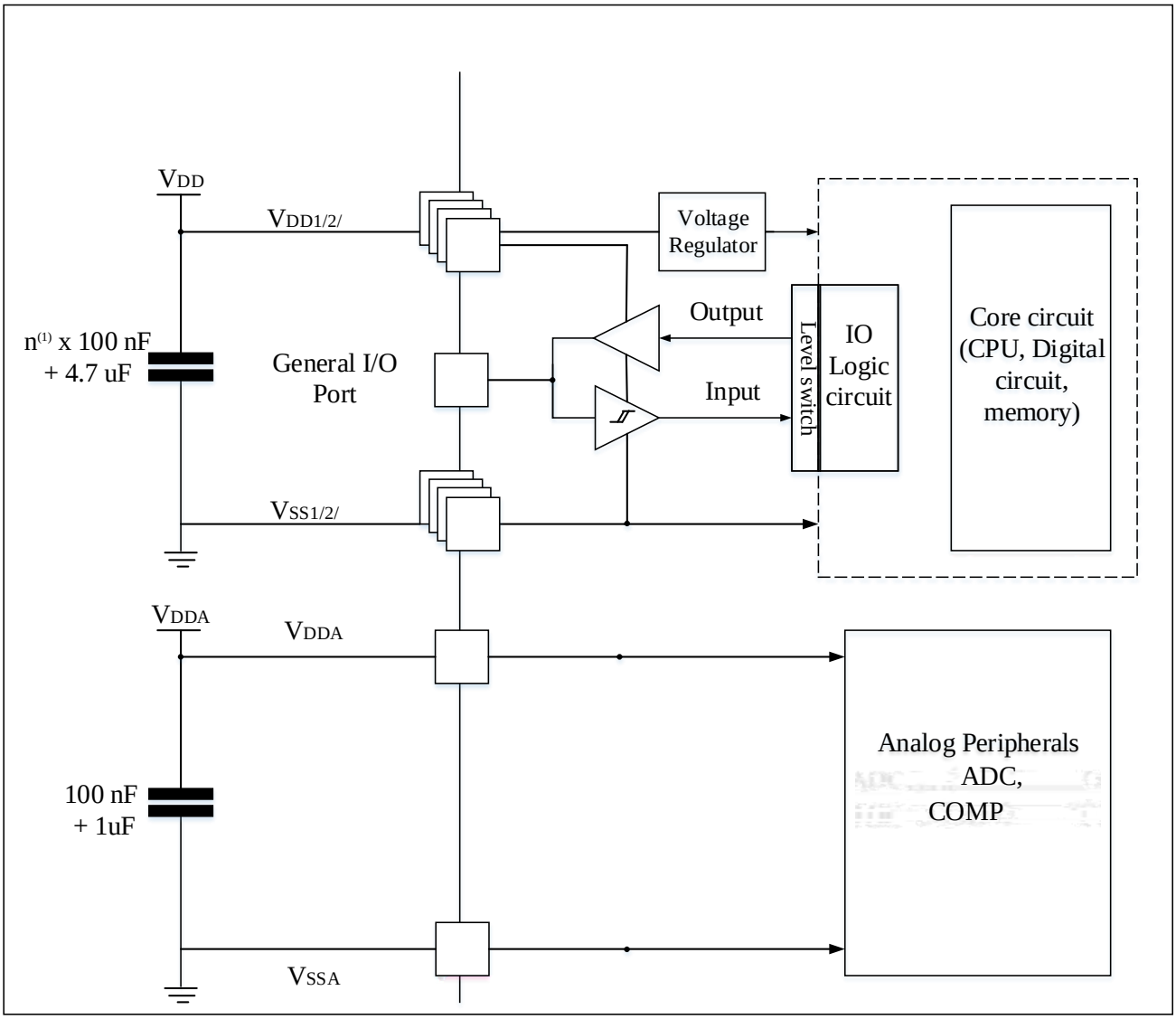
(

4-2



4.1.6

4-3



1. n V_{DD}

4.3

4.3.1

4-4

	Rising	PVD[3:0]=8	3.4	3.48	3.56	
	Falling	PVD[3:0]=8	3.3	3.38	3.46	
	Rising	PVD[3:0]=9	3.6	3.68	3.76	
	Falling	PVD[3:0]=9	3.5	3.58	3.66	
	Rising	PVD[3:0]=10	3.8	3.88		

	Rising	LVR[3:0]=13	4.4	4.48	4.56	
	Falling	LVR[3:0]=13	4.3	4.38	4.46	
	Rising	LVR[3:0]=14	4.6	4.68	4.76	
	Falling	LVR[3:0]=14	4.5	4.58	4.66	
	Rising	LVR[3:0]=15	4.8	4.88	4.96	
	Falling	LVR[3:0]=15	4.7	4.78	4.86	
$V_{LVRhyst}$(1)	LVR	-	80	100	125	mV
$V_{POR/PDR}$	VDD /	-	-	1.53	-	V
$T_{RSTTEMPO}$(1)		-	-	150		us

1.

4.3.4

4-4 V_{DD}

4-7

V_{REFINT}		- A	1.203	1.21	1.217	V
$T_{S\_vrefint}$(1)	ADC	PLS[2:0]=001 ( ) f_{ADC_CLK}=24M	-	TJg[( )(f*ł		

			8MHz	2.01	
			48MHz	4.0	
			40MHz	3.3	
			24MHz	2.51	
			8MHz	1.8	

1.

4-4

4.3.6.1 (HSI)RC

4-11 HSI (1)(2)

f_{HSI}		VDD=3.3V T_A		47.52(3)	48	

4.3.8 FLASH

T_A = -

4-14

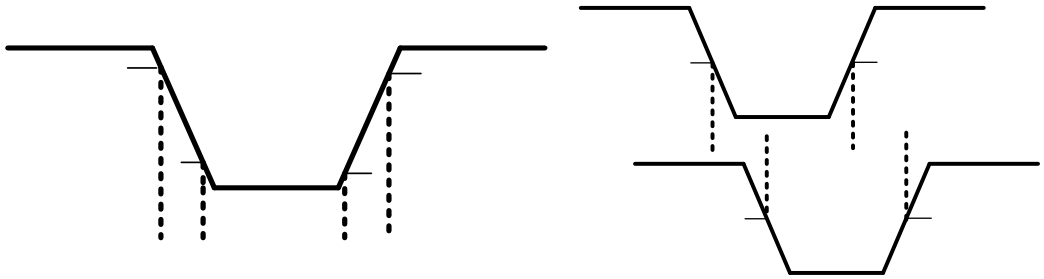
			(1)	(1)	(1)	

› t_P

	Strength	Control	CLoading(pf)						
	Low (DR=1)	Slow (SR=1)	25	2.56	3.68	6.01	3.96	5.87	9.57
			50	4.76	6.87	11.3	5.01	7.32	11.8
			100	9.24	12.2	21.9	7.46	10.7	17.1
		Fast (SR=0)	25	2.4	3.47	5.71	3.34	5	8.18

5V(4.5~5.5)

4-5



4.3.11**NRST**

NRST 4-4

4-20 NRST

		VDD				
$V_{IL(NRST)}$(1)	NRST	1.8V~5.5V	-	-	0.3VDD	V
$V_{IH(NRST)}$(1)	NRST	1.8V~5.5V	0.75VDD	-	-	
$V_{hys(NRST)}$	NRST	1.8V~5.5V				

4-6 NRST

1.

2. NRST $V_{IL(NRST)}$ MCU

4.3.12 TIM

4-21 TIMx(1)

$t_{res(TIM)}$		-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48MHz	20.8	-	ns
f_{EXT}(2)	CH1 CH4	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$= 48MHz	0	24	MHz

Res_{TIM}

4.3.14 I2C

f_{PCLK} V_{DD} 4-4

N32G003 I2C I2C SDA SCL
VDD PMOS

I2C (SDA SCL) 4.3.12

4-23 I^2C

						+		
f_{SCL}	I2C	0	100	0	400	0	1000	KHz
$t_{h(STA)}$	(1)	4.0	-	0.6	-	0.26	-	
$t_{w(SCLL)}$	SCL (1)	4.7	-	1.3	-	0.5	-	
$t_{w(SCLH)}$	SCL (1)	4.0	-	0.6	-	0.26	-	
$t_{su(STA)}$	(1)	4.7	-	0.6	-	0.26	-	
$t_{h(SDA)}$	SDA (1)	-	3.4	-	0.9	-	0.4	
$t_{su(SDA)}$	SDA (1)	250	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA SCL (1)	-	1000	20	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA SCL (1)	-	300	20	300	-	120	ns
$t_{su(STO)}$	(1)	4.0	-	0.6	-	0.26	-	
$t_{w(STO:STA)}$	( ) (1)	4.7	-	1.3	-	0.5	-	
C_b	(1)	-	400	-	400	-	100	pf
t_{SP}		0	35	0	35	0	35	ns
$t_{v(SDA)}$	(1)	3.45	-	0.9	-	0.45	-	
$t_{v\,(ACK)}$	(1)	3.45	-	0.9	-	0.45	-	

1.

2. I2C f_{PCLK} 2MHz I2C f_{PCLK}

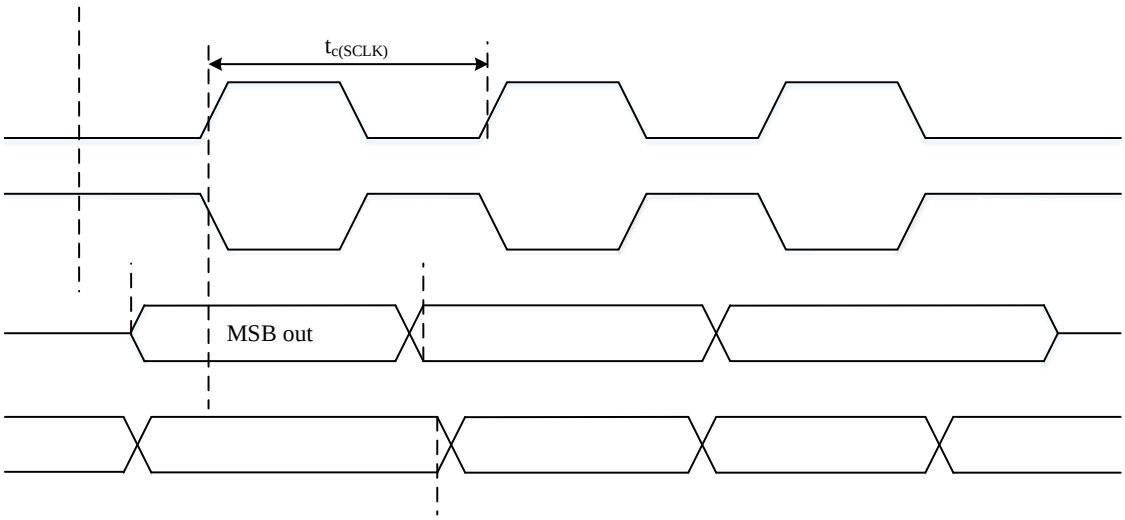
4-7

$t_{h(MI)}$(1)			5	-	ns
$t_{h(SI)}$(1)			4	-	

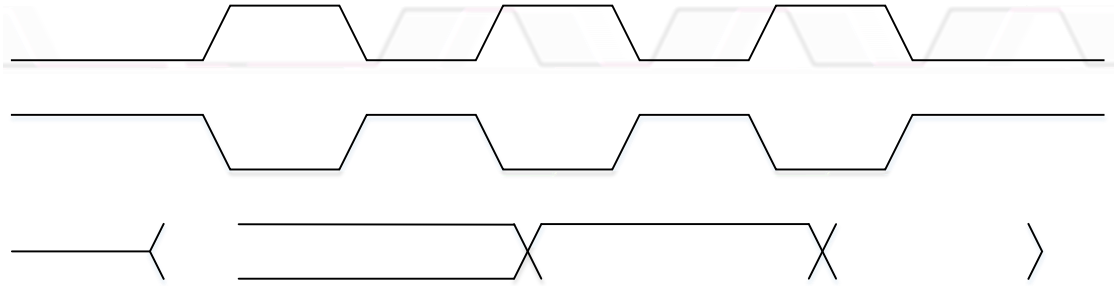
2.

3.

4-8 SPI CPHA=0

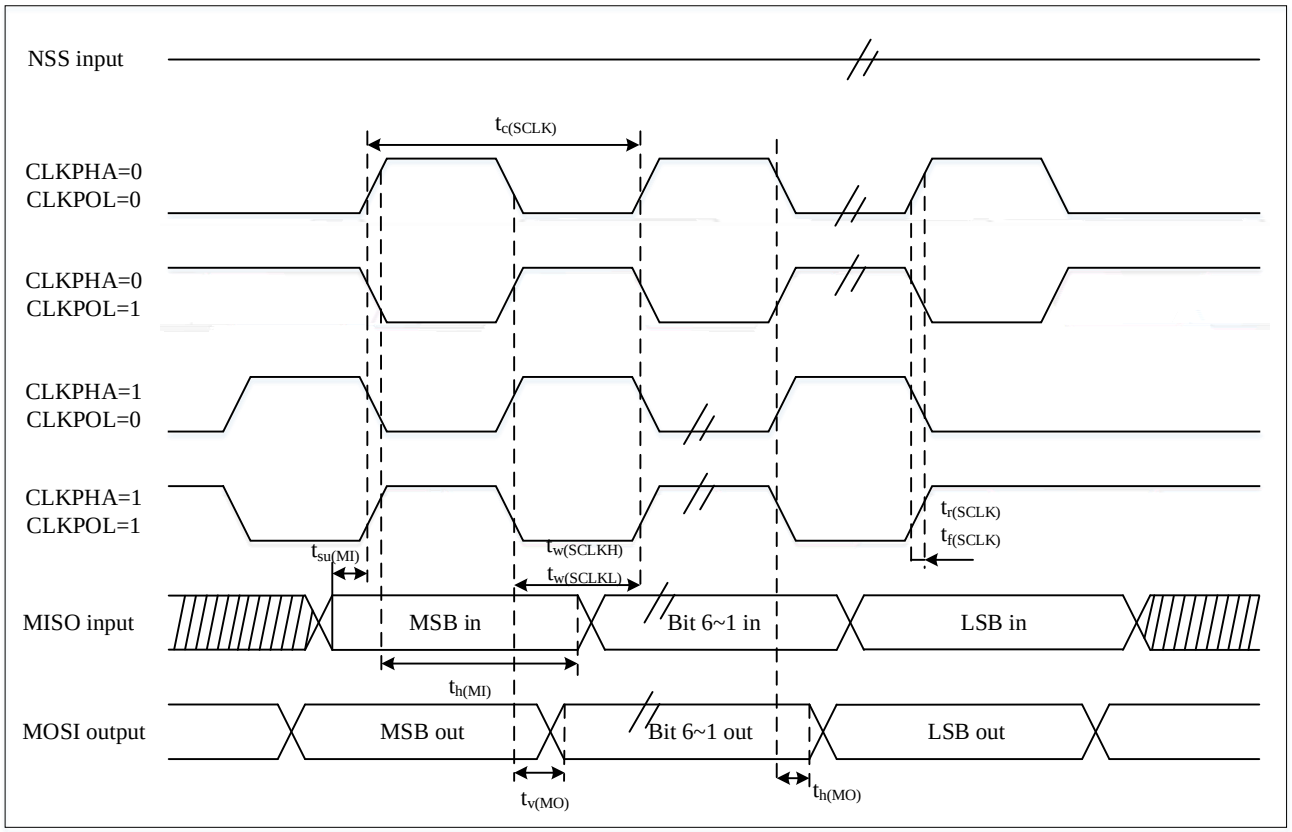


4-9 SPI CPHA=1(1)



1. CMOS 0.3V_{DD} 0.7V_{DD}

4-10 SPI (1)



1. CMOS 0.3V_{DD} 0.7V_{DD}

4.3.1612 **(ADC)**

4-25 4-4 f_{HCLK}

4-11 ADC

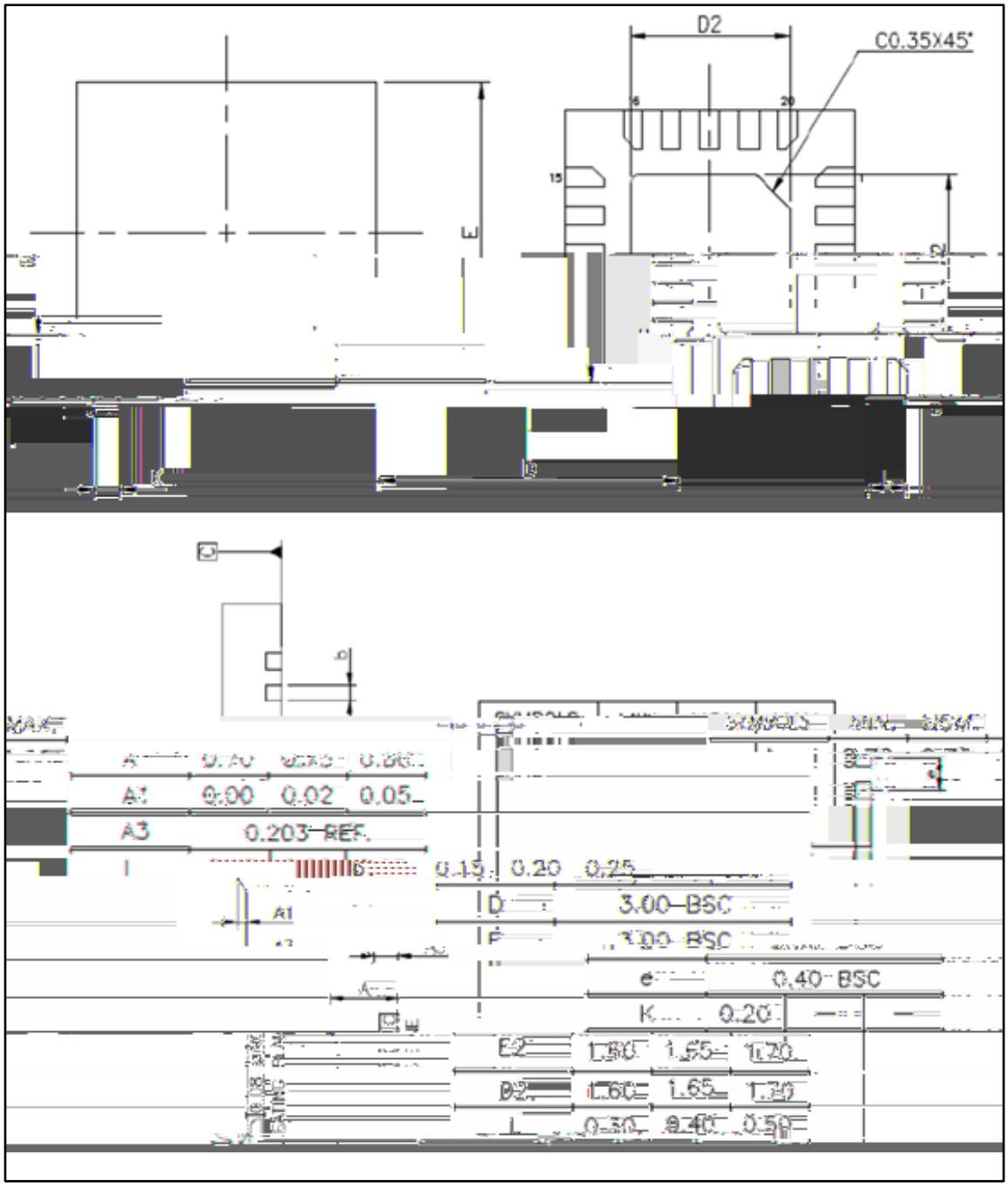
1. R_{AIN} R_{ADC} C_{ADC} 4-25
2. Cparasitic PCB(PCB) (7pF) Cparasitic f_{ADC}

4.3.17 (COMP)

5

5.1 QFN20

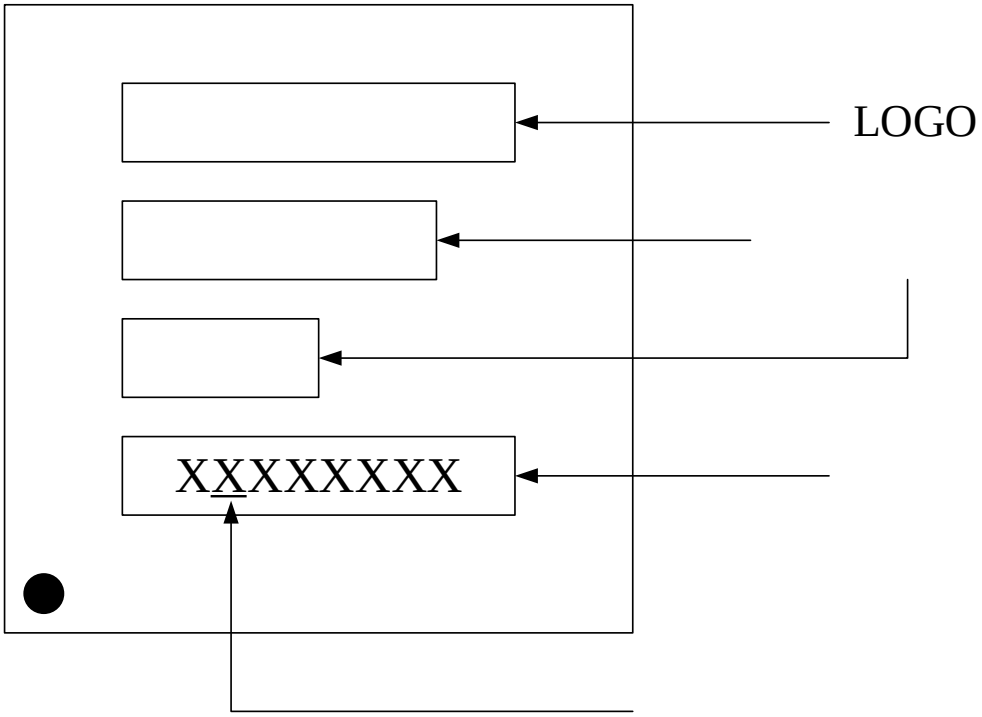
5-1 QFN20



5.2 TSSOP20

5.3

5-3



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